Amendments to the Specification:

Please replace paragraphs 23, 27, 32, 33 and 48 with the following amended paragraphs:

[0023] FIG. 2 is a partial cross-sectional view through line 2-2 of FIG. 1. In FIG. 2, wire bond pads 115 are formed on a final passivation layer 135 on a substrate 140 (which includes wires 125 (see FIG. 1), additional wires and devices such as transistors and capacitors that form the circuit of integrated circuit chip 100. Terminal passivation layer 105 overlaps edge regions 142 of wire bond pads 115. Final passivation layer 135 includes, in the present example, a first dielectric layer 145 on top of substrate 140, a second dielectric layer 150 on top of first dielectric layer 145 and a third dielectric layer 155 on top of second dielectric layer ~~155~~ 150. Terminal passivation layer 105 includes, in the present example, a first dielectric layer 160 on top of edges 142 of wire bond pads 115 and final passivation layer 135, a second dielectric layer 165 on top of first dielectric layer 160 and a third dielectric layer 170 on top of second dielectric layer 165.

[0027] FIG. 4 is a partial cross-sectional view through line 4-4 of FIG. 3. In FIG. 4, outer wire bond pads 215A and inner wire bond pads 215B are formed on a final passivation layer 235 on substrate 240 (which includes wires 225 (see FIGs. 3 and 5), additional wires and devices such as transistors and capacitors that form the circuit of integrated circuit chip 200. Final passivation layer 205 includes, in the present example, a first dielectric layer 245 on top of substrate 240, a second dielectric layer 250 on top of first dielectric layer 245 and a third dielectric layer 255 on top of second dielectric layer ~~255~~ 250. Final passivation layer 235 may include one layer, two layers, three layers as shown, or more layers. Materials and thicknesses for first dielectric layer 245, second dielectric layer 250 and third dielectric layer 255 are discussed *infra*.

[0032] FIG. 5 is a partial cross-sectional view through line 5-5 of FIG. 3. In FIG. 5, via 230 is formed through passivation layer 235 and makes physical and electrical contact to wire 225. Wire 225 is illustrated as having a core conductor 280 and a conductive liner ~~280~~ 275. In one example, core conductor 280 comprises copper and conductive liner 275 comprises layers of tantalum and tantalum nitride, the tantalum layer between the copper core and the tantalum nitride layer.

[0033] FIGs. 6A through 6J are partial cross-section views through line 4-4 of FIG. 3, illustrating fabrication of wire bond pads according to first, second and third embodiments of the present invention. In FIG. 6A, passivation layer 235 is formed on substrate 240 . Passivation layer 235 comprises first dielectric layer ~~255~~ 245, second dielectric layer ~~245~~ 250 and third dielectric layer 255 as described *supra*. In one example, first dielectric layer 245 comprises silicon nitride, second dielectric layer 250 comprises silicon oxide and third dielectric layer 255 comprises silicon nitride.

[0048] Continuing from FIG. 7B, in FIG. 7C, outer and inner wire bond pads 215A and 215B are recessed so that top surfaces 320 of outer and inner wire bond pads 215A and 215B are below top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 filling spaces 222. The structure illustrated in FIG. ~~7B~~ 7C constitutes the fifth embodiment of the present invention. Processing now terminates.